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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

jc525 U.S. PTO 09/217213 12/21/98

Atty. Dkt. No: 5500-05001 TT1915D	§
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Inventor(s): Mark I. Gardner H. Jim Fulford Derick J. Wristers	§
Title: SEMICONDUCTOR FABRICATION EMPLOYING IMPLANTATION OF EXCESS ATOMS AT THE EDGES OF A TRENCH ISOLATION STRUCTURE	§

CERTIFICATE OF EXPRESS MAIL
UNDER 37 C.F.R. §1.10

"Express Mail" mailing label number. EL091342197US
DATE OF DEPOSIT: December 21, 1998

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Assistant Commissioner for Patents
Washington, DC 20231

Roger Combs

UTILITY PATENT APPLICATION TRANSMITTAL

(For new non-provisional applications under 37 CFR § 1.53(b))

☒ Continuing Application — Divisional	of prior application No.: 08/923,181
Inventor(s) Gardner et al.	Filed: September 4, 1997
Title: Semiconductor Fabrication Employing Implantation of Excess Atoms at the Edges of a Trench Isolation Structure	Examiner: A. Mai Group/Art Unit: 2814 Assignee: Advanced Micro Devices, Inc. Recorded at Reel 8788, Frame 977

Application Elements

1. ☒ Filing Fee
   The filing fee is calculated as shown below.

Total Claims	9	-20=	0	x $22.00=	$0.00
Independent Claims	1	-3 =	0	x $82.00=	$0.00
Multiple Dependent Claims				Fee:	
				Basic Fee:	$760.00
				Assignment Fee	
				Sub-Total:	$760.00
				Reduction by 50% for Small Entity:	
				Total:	$760.00

☒ A check in the amount of $760.00 is enclosed.
The Commissioner is hereby authorized to charge any other fees which may be required or credit any overpayment to Conley, Rose, & Tayon, P.C., Deposit Account No. 03-2769/5500-05001.
One duplicate copy of this form is enclosed.

2. ☒ Specification as originally submitted including:
17 page of specification; 5 pages of claims, 1 page(s) of abstract, and informal figures 1-15 on 5 sheets.
3. ☒ Drawings
Formal Figures 1-5 on 5 sheets
4. ☒ Oath or Declaration
☐ Newly executed
☒ Copy from a prior application (see 37 C.F.R. § 1.63(d))
5. ☐ This application is filed by fewer than all the inventors named in the prior application
☐ Delete the following inventor(s) named in the prior non-provisional application:
____
☐ The inventor(s) to be deleted are set forth on a separate sheet attached hereto.
6. ☒ The entire disclosure of the prior application is considered to be part of the accompanying application and is hereby incorporated by reference herein.
7. ☐ Microfiche Computer Program (Appendix)
8. ☐ Nucleotide and/or Amino Acid Sequence Submission (if applicable, all necessary)
☐ Computer Readable copy
☐ Paper Copy (identical to computer copy)
☐ Statement verifying identity of above copies
9. ☒ Assignment Papers as filed in the prior application
10. Power of Attorney
☐ Is attached.
☒ The power of attorney appears in the original papers of the prior application.
☐ Since the power does not appear in the original papers, a copy of the power in the prior application is enclosed.
11. ☒ Information Disclosure Statement (IDS)
☒ Form PTO-1449
☐ Copies of IDS Citations
12. Amendments
☒ A preliminary amendment is enclosed.
☒ Cancel in this application claim(s) 1-17 before calculating the filing fee. At least one independent claim, Claim 18, is retained for filing purposes.
☒ Amend the specification by inserting before the first line the sentence: --This is a Division of application Serial No. 08/923,181, filed September 4, 1997.
13. ☒ Return Receipt Postcard
14. Small Entity Status
☐ A small entity statement is enclosed.
☐ A small entity statement was filed in the prior non-provisional application and such status is still proper and desired.
☐ Is no longer claimed.
15. ☐ Priority of foreign application number ________, filed on _____ in ____________ is claimed under 35 U.S.C. §§ 119(a)-(d)
16. ☐ Petition under 37 C.F.R. § 136 for Extension of Time
17. ☐ Other: ____________________________

Address all future correspondence to:
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Signature	
Name	Kevin L. Daffer
Registration No.	34,146
Date	December 21, 1998

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application. No: unknown
Filed: herewith
Inventor(s):
Gardner et al.

Title: SEMICONDUCTOR FABRICATION EMPLOYING IMPLANTATION OF EXCESS ATOMS AT THE EDGES OF A TRENCH ISOLATION STRUCTURE

Examiner: unknown
Group/Art Unit: unknown

Atty. Dkt. No: 5500-05001

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Roger Combs

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

The captioned application is a divisional application from prior application 08/923,181 filed September 4, 1997 pursuant to 37 C.F.R. § 1.53(b). Prior to initial examination of the captioned matter, please amend the case as follows:

In the Specification:

On page 7, line 18, after "barrier atoms, e.g., nitrogen," please delete "arsenic" and substitute therefor --argon--.

On page 14, line 5, after "barrier ions, e.g., nitrogen," please delete "arsenic" and substitute therefor --argon--.

In the Claims:

Please cancel claims 1-17 which were indicated as canceled in the transmittal sheet forwarded herewith. Please amend pending claim 18 and add the following claims 19-26 as follows:

18. (Amended) An isolation structure laterally disposed between a first active region and a second active region of a semiconductor substrate, comprising:

a trench formed within said semiconductor substrate;

a thermally grown oxide layer having a first portion disposed across a bottom of said trench, and second and third portions disposed within said trench laterally adjacent to said first and second active regions; [and]

a deposited oxide disposed within said trench above said first portion and between said second and third portions, said deposited oxide having an upper surface which is approximately coplanar with an upper surface of said semiconductor substrate; and

silicon atoms [implanted exclusively into] arranged within regions of said first and second active [areas] regions proximate said upper surface of said substrate and laterally adjacent to said second and third portions of said thermally grown oxide.

Please add claims 19-26 as follows:

--19. (Added) The isolation structure as recited in claim 18, wherein the silicon atoms are arranged within the first and second active regions directly beneath a spacer.--

--20. (Added) The isolation structure as recited in claim 19, wherein the spacer extends from a sidewall of a masking layer residing over the semiconductor substrate to the lateral perimeter of the trench.--

--21. (Added) The isolation structure as recited in claim 20, wherein the lateral distance between the sidewall of the masking layer and the trench, over which the spacer extends, is approximately 0.1 micron.--

--22. (Added) A semiconductor topography, comprising:

a dielectric filled trench arranged within a semiconductor substrate; and

barrier atoms arranged within the semiconductor substrate beneath a spacer that extends above a portion of the semiconductor substrate between the trench and a sidewall surface of a masking layer.--

--23. (Added) The semiconductor topography as recited in claim 22, wherein the spacer is configured laterally between a peripheral of the trench and the sidewall surface of the masking layer.--

--24. (Added) The semiconductor topography as recited in claim 22, wherein the spacer is made of a different material than the dielectric filled trench.--

--25. (Added) The semiconductor topography as recited in claim 22, wherein the barrier atoms are selected from the group consisting of nitrogen, argon and germanium, or combinations thereof.--

--26. (Added) The semiconductor topography as recited in claim 22, wherein the barrier atoms are arranged within a source or drain region of the semiconductor substrate within 0.1 micron of the trench.--

CONCLUSION

In the present Amendment, Applicants present pending claim 18 and additional claims 19-26 for consideration by the Examiner. The present Preliminary Amendment is believed to present the claims in better form for consideration. Favorable action is respectfully requested. If the Examiner has any questions, comments, or suggestions, the undersigned earnestly requests a telephone conference.

Respectfully submitted,

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Stacy Sue Sutton

SEMICONDUCTOR FABRICATION EMPLOYING IMPLANTATION OF EXCESS ATOMS AT THE EDGES OF A TRENCH ISOLATION STRUCTURE

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BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates to integrated circuit fabrication and more particularly to an improved process of implanting excess atoms within active areas of a semiconductor substrate laterally adjacent to a trench isolation structure to enhance properties of the integrated circuit.

2. Description of the Relevant Art

The fabrication of an integrated circuit involves placing numerous devices in a single semiconductor substrate. Select devices are interconnected by conductors which extend over a dielectric that separates or "isolates" those devices. Implementing an electrical path across a monolithic integrated circuit thus involves selectively connecting devices which are isolated from each other. When fabricating integrated circuits it is therefore necessary to isolate devices built into the substrate from one another. From this perspective, isolation technology is one of the critical aspects of fabricating a functional integrated circuit.

A popular isolation technology used for a MOS integrated circuit involves the process of locally oxidizing silicon. Local oxidation of silicon, or LOCOS processing involves oxidizing field regions of a silicon-based substrate between device areas. The oxide grown in the field or isolation regions is termed "field oxide". The field oxide is grown during the initial stages of integrated circuit fabrication, before source and drain implants are placed in device areas or active areas. By growing a thick field oxide in field regions pre-implanted with a channel-stop dopant, LOCOS processing serves to prevent the establishment of parasitic channels in the field regions.

While LOCOS has remained a popular isolation technology, there are several problems associated with LOCOS. First, a growing field oxide extends laterally as a bird's-beak structure. In many instances, the bird's-beak structure can unacceptably encroach into the device active area. Second, the pre-implanted channel-stop dopant redistributes during the high temperatures associated with field oxide growth. Redistribution of channel-stop dopant primarily affects the active area periphery, causing problems known as narrow-width effects. Third, the thickness of field oxide causes large elevational disparities across the semiconductor topography between field and active regions. Topographical disparities cause planarity problems which become severe as circuit critical dimensions shrink. Lastly, thermal oxide growth is significantly thinner in small field regions(*i.e.*, field areas of small lateral dimension) relative to large field regions. In small field regions, a phenomenon known as field-oxide-thinning effect therefore occurs. Field-oxide-thinning produces problems with respect to field threshold voltages, interconnect-to-substrate capacitance, and field-edge leakage in small field regions between closely spaced active areas.

Many of the problems associated with LOCOS technology are alleviated by an isolation technique known as the "shallow trench process". The shallow trench process is particularly suited for isolating densely spaced active devices having field regions less than one micron in lateral dimension. Conventional trench processes involve the steps of etching a silicon substrate surface to a relatively shallow depth, *e.g.*, between 0.2 to 0.5 microns, and then refilling the shallow trench with a deposited dielectric. The trench is then planarized to complete formation of the isolation structure. The trench process eliminates bird's-beak and channel-stop dopant redistribution problems. In addition, the isolation structure is fully recessed, offering at least a potential for a planar surface. Still further, field-oxide thinning is reduced in narrow isolation spaces, and the threshold voltage is constant as a function of channel width.

While the conventional trench isolation process has many advantages over LOCOS, the trench process also has problems. Because trench formation involves

etching of the silicon substrate, it is believed that dangling bonds and an irregular grain structure form in the silicon substrate near the walls of the trench. Such dangling bonds may promote trapping of charge carriers within the active areas of an operating transistor. As a result, charge carrier mobility may be hindered, and the output current, I_D, of the transistor may decrease to an amount at which optimum device performance is unattainable.

Further, during subsequent anneal steps (e.g., thermal oxidation for gate oxide formation), the irregular grain structure may provide migration avenues through which oxygen atoms can pass from the trench isolation structures to the active areas. Moreover, the dangling bonds may provide opportune bond sites for diffusing oxygen atoms, thereby promoting accumulation of oxygen atoms in the active areas near the edges of the isolation structures. It is believed that oxygen atoms present in active areas of the silicon may function as electron donors. Thus, inversion of subsequently formed p-type active areas may undesirably occur near the walls of the isolation trench. Further, the edge of a device may conduct less current than the interior portion of the device. Therefore, more charge to the gate of a transistor may be required to invert the channel, causing threshold voltage, V_T, to shift undesirably from its design specification.

It is postulated that during the growth of a gate oxide across regions of the substrate exclusive of the isolation regions, the presence of foreign oxygen atoms at the surface of the silicon crystal lattice may lead to a relatively high defect density in the gate oxide. It is further postulated that foreign oxygen atoms accumulating within the active areas may result in regions of the substrate having a high defect density. For example, clusters of foreign atoms may cause dislocations to form in the substrate. It is also believed that low breakdown voltages in thin gate oxides correlate with high defect density near the surface of the substrate.

In a subsequent processing step, the active areas of the semiconductor substrate may be implanted with impurity species to form source/drain regions therein. The

semiconductor topography may be subjected to a high temperature anneal to activate the impurity species in the active areas and to annihilate crystalline defect damage of the substrate. Unfortunately, impurity species which have a relatively high diffusivity, such as boron, may undergo diffusion into the isolation region when subjected to high temperatures. As a result, the threshold voltage in the isolation region may decrease and current may inadvertently flow (i.e., leakage) between isolated active areas.

It is therefore desirable to develop a technique for forming a trench isolation structure between active areas in which problems related to dangling bonds and to an irregular grain structure at the edges of the active areas are alleviated. Such a technique is necessary to inhibit charge carriers and oxygen donors from being entrapped in the active areas. It is also necessary that the trench isolation technique provide for the growth of a high quality gate oxide which does not easily undergo breakdown. Yet further, it is desirable that inversion of silicon within the active areas near the edges of the trench isolation structures be prevented.

SUMMARY OF THE INVENTION

The problems noted above are in large part solved by the method hereof for isolating active areas within a semiconductor substrate. That is, the present invention contemplates the formation of a trench isolation structure between active areas of a semiconductor substrate. Advantageously, excess atoms are incorporated in the active areas adjacent to the walls of the trench to enhance the properties of both the isolation structure and of devices employing the active areas. Herein, excess atoms may be silicon atoms in addition to the atoms of the single crystalline silicon substrate or other impurity atoms.

According to an embodiment of the present invention, a semiconductor topography is provided in which a masking layer is formed above a semiconductor substrate. An opening is formed vertically through the masking layer, and a dielectric spacer material is deposited across the exposed surface of the topography. The spacer material is then anisotropically etched to form spacers directly adjacent to opposed sidewall surfaces of the masking layer opening. The spacers are strategically placed above regions of the substrate into which excess atoms are to be subsequently implanted. An isolation trench is then etched into the semiconductor substrate between the spacers. The resulting trench is relatively shallow and is interposed between ensuing active areas of the semiconductor substrate.

An oxide (i.e., SiO_2) layer may be thermally grown within the trench on the exposed edges of the substrate. Oxide may then be deposited using chemical vapor deposition ("CVD") into the trench and across the masking layer surface. Chemical-mechanical polishing ("CMP") may be used to planarize the upper surface of the masking layer. The oxide may then be etched down to an elevation commensurate with the upper surface of the semiconductor substrate. The spacers may be concurrently etched down to near the surface of the substrate. The resulting trench isolation region includes both a thermally grown oxide and a deposited oxide. As described previously, a

shallow isolation trench which is filled with a deposited oxide has many benefits over LOCOS isolation structures. However, deposited oxide is generally less dense than thermally grown oxide and has an altered stoichiometry that can cause changes in the mechanical and electrical properties of the film. Thermally grown oxide, on the other hand, has a generally uniform stoichiometry arrangement which provides for consistent electrical isolation. Accordingly, thermally grown oxide is strategically arranged at the periphery of the trench adjacent to the active areas which require electrical isolation. The remaining bulk of the isolation structure is CVD oxide.

Ion implantation may then be performed to implant silicon atoms into exposed areas of the semiconductor topography, particularly into areas of the semiconductor substrate directly under the spacers and adjacent to the walls of the trench. Acceleration of the ions may be controlled so as to move the ions into those critical areas of the substrate. The masking layer thickness is pre-selected to prevent the ions from passing into the regions of the semiconductor substrate directly under the masking layer. The masking layer and any remaining portions of the spacers are removed in preparation for the growth of a gate oxide across the substrate.

Silicon atoms thusly placed in the semiconductor substrate may contribute many useful features to active area isolation. They may fill vacancies and interstitial sites within the silicon crystal lattice. Thus, the silicon atoms may "stuff" grain-boundary diffusion pathways into and out of the active areas, thereby preventing cross-diffusion of impurities between the isolation structures and the active areas. As a result, problems associated with these occurrences, such as current leakage between active areas and edge inversion of a transistor may be reduced. Furthermore, the silicon atoms may promote the formation of a high quality salicide above regions of the active areas incorporated with the excess silicon atoms. Salicide, i.e., self-aligned silicide, formation above active areas of transistors is a well known technique. During salicide formation, metal atoms are reacted with silicon atoms at the surface of the substrate. Since the presence of excess silicon atoms in the active areas helps prevent impurity atoms from entering the

active areas, such impurity atoms may also be inhibited from being incorporated in the salicide. The resulting salicide may thus be free of such impurities.

Moreover, it is believed that the growth rate of a thermally grown oxide at the surface of the substrate above those regions densely packed with silicon atoms is increased. Thus, a thicker gate oxide may be formed above regions of the substrate adjacent to the edges of the trench isolation structure. The formation of a thicker gate oxide in these regions may cause the threshold voltage at the edges of the active areas to increase such that edge inversion of operating transistors is prevented. Since the gate oxide thickness above other regions of the substrate is kept relatively thin, the threshold voltage of transistors employing the active areas may be maintained at its desired value. Yet further, the growth of a thicker gate oxide advantageously raises the breakdown voltage of the oxide, making oxide breakdown less likely. It is also believed that since the silicon atoms help inhibit oxygen atoms from entering the active areas and becoming entrapped by dangling bonds, defect density of an oxide grown above the active areas is reduced.

In an alternate embodiment, barrier atoms, e.g., nitrogen, arsenic, or germanium atoms, instead of silicon atoms may be implanted into those regions of the active areas disposed under the spacers and adjacent to the trench isolation structure. Thusly placed, barrier atoms may fill voids in an irregular grain structure which could have resulted when etching the trench. If nitrogen barrier atoms are implanted, they may bond with available silicon atoms such that opportune bond sites no longer exist within the active areas. Further, the barrier atoms may fill interstitial sites between silicon atoms. Thus, barrier atoms may block grain-boundary diffusion pathways into and out of the active areas. Therefore, impurities are inhibited from passing into the trench isolation structure and oxygen atoms are inhibited from passing into the active areas. Therefore, current leakage between active areas and edge inversion of a transistor may be prevented. Moreover, charge carrier entrapment in the active areas may be reduced since barrier atoms have terminated many of the dangling bonds. Since Si-N bonds are stronger and

less strained than Si-O bonds, nitrogen barrier atoms are better suited for inhibiting the immobility of charge carriers near the edges of a transistor.

In yet another embodiment, both silicon atoms and nitrogen atoms may be implanted into regions of the active areas adjacent the isolation structure. Many of the benefits of using silicon atoms and nitrogen atoms individually also apply when both are used. The nitrogen atoms may, however, counter the effect that the silicon atoms have on the growth of a gate oxide at the surface of the substrate. Thus, the growth of the gate oxide might be no faster above these implanted regions than above the other regions of the substrate.

BRIEF DESCRIPTION OF THE DRAWINGS

Other objects and advantages of the invention will become apparent upon reading the following detailed description and upon reference to the accompanying drawings in which:

Fig. 1 is a partial cross-sectional view of a semiconductor topography, wherein an oxide layer is grown across a semiconductor substrate;

Fig. 2 is a cross-sectional view of the semiconductor topography, wherein a dielectric masking layer is deposited across the oxide layer, subsequent to the step in Fig. 1;

Fig. 3 is a cross-sectional view of the semiconductor topography, wherein an opening is etched vertically through the masking layer and partially through the oxide layer, subsequent to the step in Fig. 2;

Fig. 4 is a cross-sectional view of the semiconductor topography, wherein a dielectric material is deposited across the exposed surface of the topography, subsequent to the step in Fig. 3;

Fig. 5 is a cross-sectional view of the semiconductor topography, wherein the dielectric material is anisotropically etched to form spacers adjacent to sidewalls of the masking layer opening, subsequent to the step in Fig. 4;

Fig. 6 is a cross-sectional view of the semiconductor topography, wherein a trench is etched in a region of the substrate defined between the spacers, subsequent to the step in Fig. 5;

Fig. 7 is a cross-sectional view of the semiconductor topography, wherein a channel-stop implant is forwarded into a region of the substrate underlying the trench, subsequent to the step in Fig. 6;

Fig. 8 is a cross-sectional view of the semiconductor topography, wherein a layer of oxide is thermally grown across the walls and the base of the trench, subsequent to the step in Fig. 7;

Fig. 9 is a cross-sectional view of the semiconductor topography, wherein a dielectric is deposited across the topography up to an elevation which is a spaced distance above the surface of the masking layer, subsequent to the step in Fig. 8;

Fig. 10 is a cross-sectional view of the semiconductor topography, wherein the deposited dielectric is concurrently planarized and removed down to an elevation near the surface of the masking layer, subsequent to the step in Fig. 9;

Fig. 11 is a cross-sectional view of the semiconductor topography, wherein the deposited dielectric and the spacers are etched such that the upper surface of the dielectric is level with the surface of the substrate, subsequent to the step in Fig. 10;

Fig. 12a is a cross-sectional view of the semiconductor topography, wherein excess atoms are incorporated into regions of the topography using ion implantation, subsequent to the step in Fig. 11;

Fig. 12b is a detailed view along section 30 of Fig. 12a, wherein the excess atoms are shown as being incorporated into active areas of the substrate laterally adjacent to the isolation trench structure;

Fig. 13 is a cross-sectional view of the semiconductor topography, wherein the masking layer, the oxide layer, and the spacers are removed from the upper surface of the substrate, subsequent to the step in Fig. 12a;

Fig. 14 is a cross-sectional view of the semiconductor topography, wherein a gate oxide is grown across the surface of the semiconductor substrate, subsequent the step in Fig. 13; and

Fig. 15 is a cross-sectional view of the semiconductor topography, wherein a transistor is formed adjacent to the isolation trench structure and a local interconnect is formed which is coupled to a junction of the transistor.

DETAILED DESCRIPTION OF THE INVENTION

Turning now to the drawings, Fig. 1 depicts a semiconductor substrate 10 across which a thin layer of thermally grown oxide 12 is disposed. Semiconductor substrate 10 comprises single crystalline silicon. As shown in Fig. 2, a dielectric masking layer 14, preferably nitride (Si_3N_4), may be deposited across oxide layer 12. The nitride deposition may be performed using, e.g., a horizontal tube LPCVD reactor. Oxide layer 12 is a "pad oxide" which reduces inherent stresses that exist between CVD nitride on silicon. Fig. 3 depicts the etching of a contiguous opening 16 through masking layer 14 and partially through oxide layer 12. A dry, plasma etch technique may be used to form opening 16 in which etch duration is chosen to terminate just before reaching the surface of substrate 10. It is also possible to etch through the entire thickness of oxide layer 12, but overetching may result in unwanted removal of the underlying substrate 10.

Fig. 4 illustrates the chemical vapor deposition of a dielectric material 18, e.g., oxide, nitride, or oxynitride, across the exposed surfaces of masking layer 14 and oxide layer 12. Dielectric material 18 may be anisotropically etched to form spacers 20 which are depicted in Fig. 5. Since anisotropic etch removes material at a faster rate vertically than horizontally, etch duration is chosen to terminate before bombarding etchant ions may attack a predetermined thickness of the dielectric material disposed immediately adjacent to the sidewall surfaces of masking layer 14. Preferably the thickness of each of the remaining spacers 20 is about 0.1 micron in the lateral (horizontal) direction.

Turning to Fig. 6, a trench 22 may be anisotropically etched in a region of substrate 10 defined between spacers 20. Prior to etching substrate 10, a photoresist masking layer (not shown) may be patterned directly above masking layer 14 and spacers 20 using well known optical lithography techniques to prevent removal of these structures during the etch process. Fig. 7 depicts dopants being implanted into a region 24 of substrate 10 directly below trench 22. Masking layer 14 and spacers 20 prevent implants from entering material beneath those regions. Only the trench 24, exposed

between spacers 20, receives the blanket implant. This implant is performed to create a channel-stop doping layer under the ensuing field oxide. The type of dopants chosen for the channel-stop implant is opposite to that used during a later implant into active areas 25 which are separated by trench 22. A p^+ implant of boron or an n^+ implant of arsenic may, e.g., be used.

As shown in Fig. 8, the semiconductor topography is then exposed to thermal radiation 27, resulting in the oxidation of exposed silicon within substrate 10. A thermally grown oxide layer 24 is thusly formed which lines the walls and the base of trench 22. Fig. 9 depicts the deposition of a fill dielectric material 26, e.g., CVD oxide into trench 22. The fill oxide 26 is deposited until the upper surface of the material is at an elevation above the surface of masking layer 14. Subsequently, chemical-mechanical polishing (CMP), or a combination of etchback and/or CMP, may be used to simultaneously planarize the upper surface of fill oxide 26 and remove the material down to an elevation proximate the peaks of spacers 20.

Turning to Fig. 11, fill oxide 26 may then be etched such that its upper surface is commensurate with the surface of substrate 10. A photoresist masking layer may be patterned above masking layer 14 to prevent removal of masking layer 14 during the etch process. Fill oxide 26 combined with oxide layer 24 form a trench isolation structure. Spacers 20 are concurrently etched along with fill oxide 26 such that they each have a thickness of between 0 to 200 Å, depending on the etch process used and the type of spacer material. For example, if a dry, plasma etch which has low selectivity relative to oxide is used to etch fill oxide 26, almost all of spacers 20 may be removed. A large portion of spacers 20 may also be removed using an etch step that is highly selective to oxide if the spacers are composed of oxide. Conversely, if spacers 20 are made of oxynitride or nitride and an etch technique which is highly selective to oxide is performed, less of the spacers 20 may be removed. Nitride spacers would be thicker than oxynitride spacers after an oxide selective etch, e.g., a wet etch process using a hydrofluoric acid solution. A relatively short or thin residual spacer is deemed important

in allowing barrier atom ingress into the substrate directly beneath the barrier, as described below.

As depicted in Fig. 12a, silicon ions may be implanted into the semiconductor topography. In addition to the silicon ions, barrier ions, e.g. nitrogen, argon arsenic or germanium ions may also be forwarded to the topography using ion implantation. Alternately, only barrier ions and no silicon ions may be implanted. The use of ion implantation provides for tight control of the depth at which the excess atoms come to reside. Ion acceleration is chosen so as to incorporate excess silicon and/or barrier atoms into regions 28 of substrate 10. Masking layer 14 inhibits the excess atoms from passing to other regions of substrate 10. The excess atoms may also become implanted near the surface of the trench isolation structure. Spacers 20 are strategically disposed above regions 28 and between masking layer 14 and the trench isolation structure. Since a large portion of spacers 20 have been removed from the sidewalls of masking layer 14, the ions may be forwarded through the relatively thin spacers 20 to regions 28 which are disposed in close proximity to the trench isolation structure.

Fig. 12b depicts a detailed view along section 30 of Fig. 12a. Active area 15 may form a source and drain region of a transistor in subsequent processing steps. Silicon atoms 32 and/or nitrogen atoms 34 are shown as being incorporated in close proximity to the thermal oxide 24/ active area 15 interface. The implanted atoms may fill vacancies and interstitial sites within the silicon crystal lattice of active area 15. Thus, in subsequent processing when the semiconductor topography is exposed to heat, silicon atoms 32 and/or nitrogen atoms 34 may block or "stuff" migration pathways of oxygen atoms 35 from the isolation structure into active area 15. The excess atoms may also block impurity species in active area 15 from passing to the trench isolation structure. Further, Si-N bonds which are relatively strong may form, reducing the possibility of species such as charge carriers becoming trapped by dangling bonds. As shown later, silicon atoms 32 may also increase the growth rate of a thermally grown oxide at the surface of region 28.

After incorporating nitrogen atoms into regions 28 of active areas 15, the semiconductor topography undergoes preparation for subsequent formation of transistors which are to be isolated from each other by the trench isolation structure. As shown in Fig. 13, masking layer 14, spacers 20, and oxide layer 12 may be etched away. They may be removed using, e.g., various wet etch techniques. For instance, if masking layer 14 and spacers 20 are composed of nitride, these structures may be etched using reflux boiled phosphoric acid. Oxide layer 12 may then be removed using a hydrofluoric acid solution as the etchant. After cleaning any contaminants from the surface of the semiconductor topography, a gate oxide 38 may be grown across the surface, as shown in Fig. 14. Exposure of the topography to thermal radiation 36 is used to promote the oxidation of the silicon at the surface of substrate 10. As mentioned earlier, if regions 28 include excess silicon atoms, the oxide growth rate above these regions may be faster than above other areas of the substrate. Thus, the gate oxide 38 may be thicker above regions 28.

Turning to Fig. 15, source/drain ("S/D") regions 42 are shown as being formed in the active areas of substrate 10, according to one embodiment. The formation of S/D regions 42 may involve implanting dopants into areas of the substrate not covered by a masking layer. A region of gate oxide 38 is exclusively etched away using e.g., a wet oxide etch to expose a portion of one of the S/D regions 42. A polysilicon layer may then be deposited across the surface of the semiconductor topography. Portions of the polysilicon may be etched away and doped to form a gate conductor 40 between S/D regions 42 and a local interconnect 44 coupled to one of the S/D regions. Gate oxide 38 is maintained beneath interconnect 44 so as to electrically isolate local interconnect 44 from all other electrically active areas. Local interconnect 44 may extend a relatively short distance to a gate or S/D region of another transistor. Local interconnect 44 may also be made of other materials, such as metals. The active areas isolated by the method hereof may also be used to form transistors to which dielectrically isolated contacts can be formed. Interconnects dielectrically isolated above the transistors may be formed

between different contacts, thereby placing certain active areas in electrical communication with each other.

It will be appreciated to those skilled in the art having the benefit of this disclosure that this invention is believed to provide a method for forming actives areas isolated from each other by a trench isolation structure in which the isolation structure and devices employing the active areas have enhanced properties. It is intended that the following claims be interpreted to embrace all such modifications and changes and, accordingly, the specification and drawings are to be regarded in an illustrative rather than a restrictive sense.

WHAT IS CLAIMED IS:

1. A method for forming a trench isolation region, comprising:

providing a semiconductor topography comprising a masking layer disposed above a semiconductor substrate, wherein an opening is formed vertically through said masking layer;

forming first and second dielectric spacers laterally adjacent to opposed sidewall surfaces of said opening;

etching a trench within said substrate between said first and second dielectric spacers;

forming dielectric material within said trench and said opening;

removing portions of said dielectric material and portions of said first and second dielectric spacers such that an upper surface of said dielectric material is approximately commensurate with an upper surface of said substrate; and

implanting silicon atoms in areas of said substrate directly beneath said first and second spacers and laterally adjacent to sidewalls of said trench.

2. The method of claim 1, wherein said masking layer comprises silicon nitride, and wherein said semiconductor topography further comprises an oxide layer interposed between said semiconductor substrate and said masking layer, and wherein said opening extends at least partially through said oxide layer.

3. The method of claim 1, wherein the step of forming said first and second dielectric spacers comprises:

depositing an insulative layer across exposed surfaces of said masking layer and said opening; and

etching said insulative layer at a greater rate perpendicular to said semiconductor substrate than parallel to said semiconductor substrate to form said first and second dielectric spacers.

4. The method of claim 3, wherein said insulative layer comprises a material selected from the group consisting of oxide, nitride, and oxynitride.

5. The method of claim 1, further comprising implanting dopants into an exposed region of said substrate directly under said trench prior to the step of forming said dielectric material in said trench and said opening.

6. The method of claim 1, wherein the step of forming said dielectric material in said trench and said opening comprises:

thermally growing an oxide layer in said trench on exposed regions of said semiconductor substrate;

depositing a fill oxide across said masking layer and into said opening and said trench; and

chemical-mechanical polishing said fill oxide to an elevational level directly below an upper surface of said masking layer.

7. The method of claim 1, wherein each of said first and second dielectric spacers comprises a width of about 0.1 micron.

8. The method of claim 1, wherein the step of removing said portions of said dielectric material and said first and second spacers comprises (i) forming a photoresist layer exclusively above said masking layer and (ii) plasma etching or wet etching said portions of said dielectric material and said first and second spacers such that said first and second spacers are about 0 to 200 Å thick.

9. The method of claim 1, further comprising removing said first and second nitride spacers and said masking layer, subsequent to the step of incorporating said silicon atoms.

10. The method of claim 1, wherein said areas of said substrate are portions of active regions of said semiconductor substrate.

11. The method of claim 1, further comprising thermally growing a gate oxide across said semiconductor substrate, wherein said gate oxide comprises a first thickness above said areas and a second thickness above regions of said substrate exclusive of said areas, and wherein said first thickness is greater than said second thickness.

12. The method of claim 1, further comprising implanting nitrogen atoms in said areas of said substrate directly under said first and second spacers and laterally adjacent to said sidewalls of said trench.

13. A method for forming a trench isolation region, comprising:

providing a semiconductor topography comprising a masking layer disposed above a semiconductor substrate, wherein an opening is formed vertically through said masking layer;

forming first and second dielectric spacers laterally adjacent to opposed sidewall surfaces of said opening;

etching a trench within said substrate between said first and second dielectric spacers;

forming dielectric material within said trench and said opening;

removing portions of said dielectric material and portions of said first and second dielectric spacers such that an upper surface of said dielectric material is approximately commensurate with an upper surface of said substrate; and

implanting barrier atoms in areas of said substrate directly beneath said first and second spacers and laterally adjacent to sidewalls of said trench.

14. The method of claim 13, wherein said barrier atoms comprise atoms selected from the group consisting of nitrogen atoms, argon atoms, and germanium atoms or combinations thereof.

15. The method of claim 13, wherein the step of forming said dielectric material in said trench and said opening comprises:

thermally growing an oxide layer in said trench on exposed regions of said semiconductor substrate;

depositing a fill oxide across said masking layer and into said opening and said trench; and

chemical-mechanical polishing said fill oxide to an elevational level directly below an upper surface of said masking layer.

16. The method of claim 13, wherein each of said first and second dielectric spacers comprises a width of about 0.1 micron.

17. The method of claim 13, wherein the step of removing said portions of said dielectric material and said first and second spacers comprises (i) forming a photoresist layer exclusively above said masking layer and (ii) plasma etching or wet etching said portions of said dielectric material and said first and second spacers such that said first and second spacers are about 0 to 200 Å thick.

18. An isolation structure laterally disposed between a first active region and a second active region of a semiconductor substrate, comprising:

a trench formed within said semiconductor substrate;

a thermally grown oxide layer having a first portion disposed across a bottom of said trench and second and third portions disposed within said trench laterally adjacent to said first and second active regions; and

a deposited oxide disposed within said trench above said first portion and between said second and third portions, said deposited oxide having an upper surface which is approximately coplanar with an upper surface of said semiconductor substrate; and

silicon atoms implanted exclusively into regions of said first and second active areas proximate said upper surface of said substrate and laterally adjacent to said second and third portions of said thermally grown oxide.

ABSTRACT

A method for isolating a first active region from a second active region, both of which are configured within a semiconductor substrate. The method comprises forming a dielectric masking layer above a semiconductor substrate. An opening is then formed through the masking layer. A pair of dielectric spacers are formed upon the sidewalls of the masking layer within the opening. A trench is then etched in the semiconductor substrate between the dielectric spacers. A first dielectric layer is then thermally grown on the walls and base of the trench. A CVD oxide is deposited into the trench and processed such that the upper surface of the CVD oxide is commensurate with the substrate surface. Portions of the spacers are also removed such that the thickness of the spacers is between about 0 to 200 Å. Silicon atoms and/or barrier atoms, such as nitrogen atoms, are then implanted ino regions of the active areas in close proximity to the trench isolation structure.

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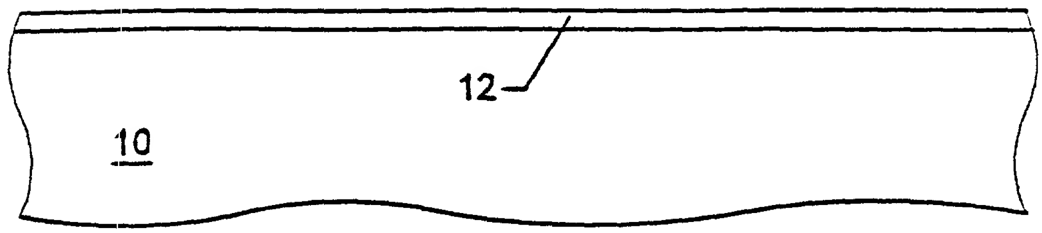

FIG. 1

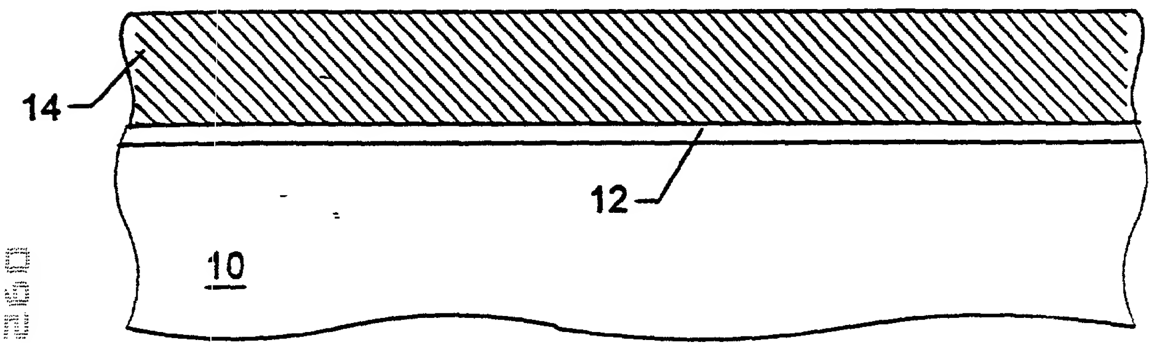

FIG. 2

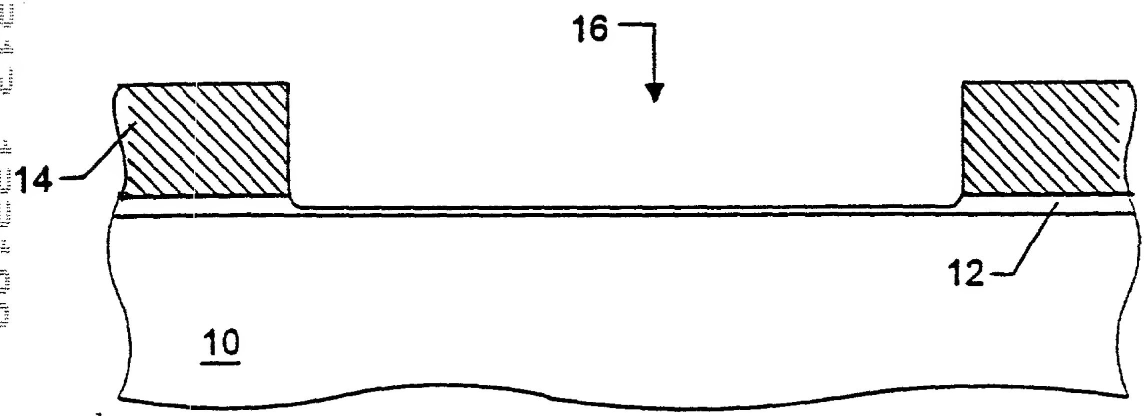

FIG. 3

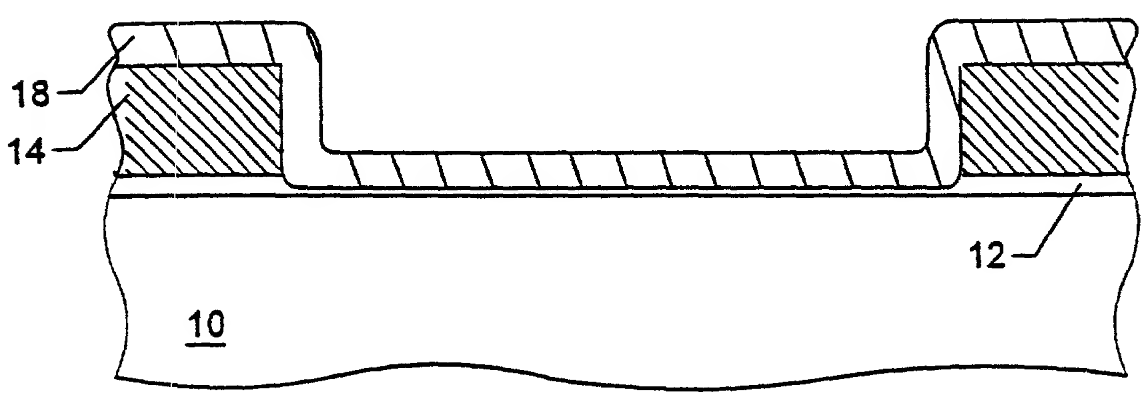

FIG. 4

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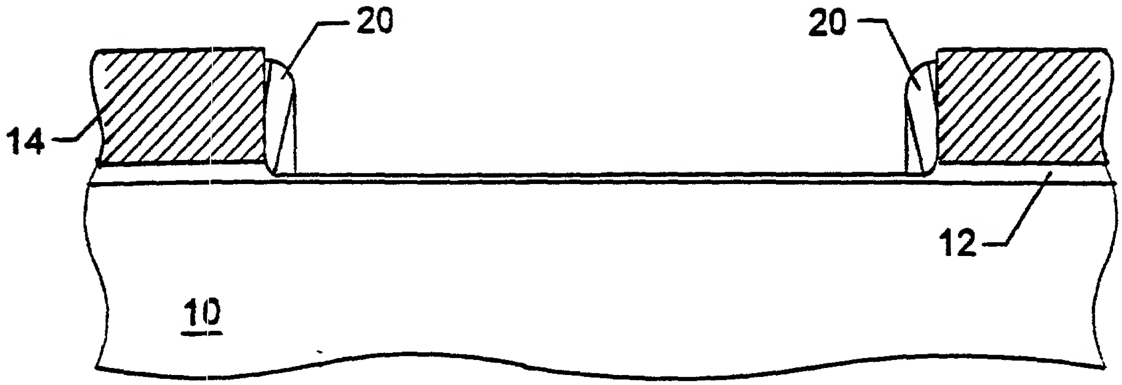

FIG. 5

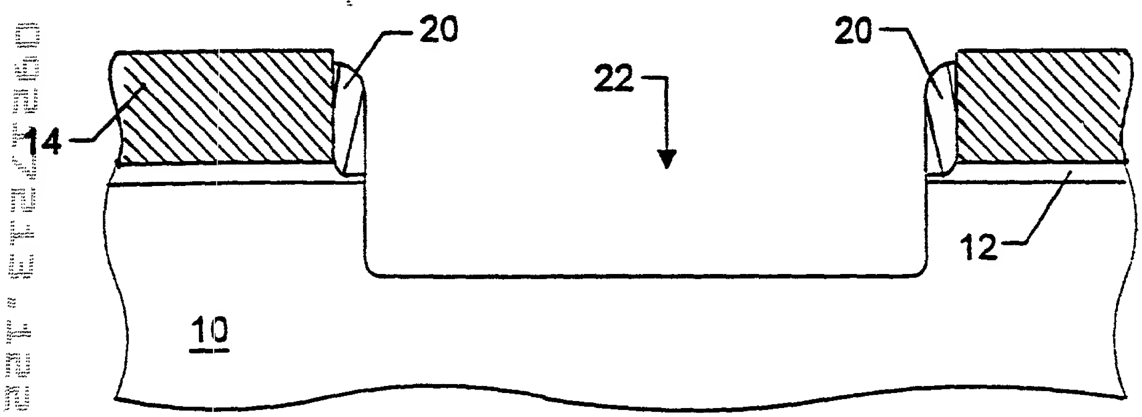

FIG. 6

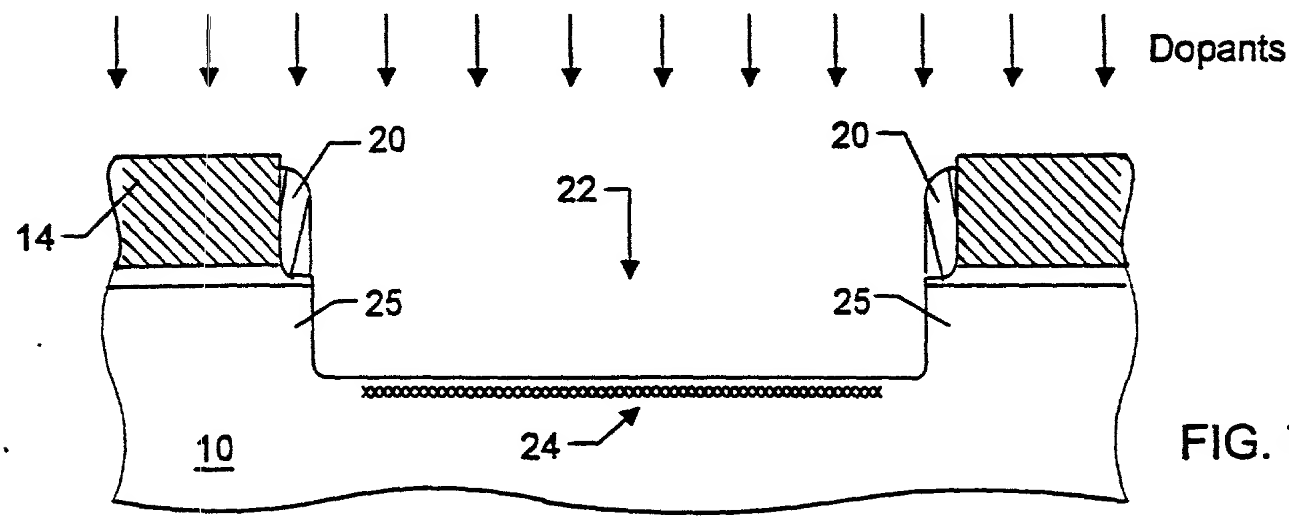

FIG. 7

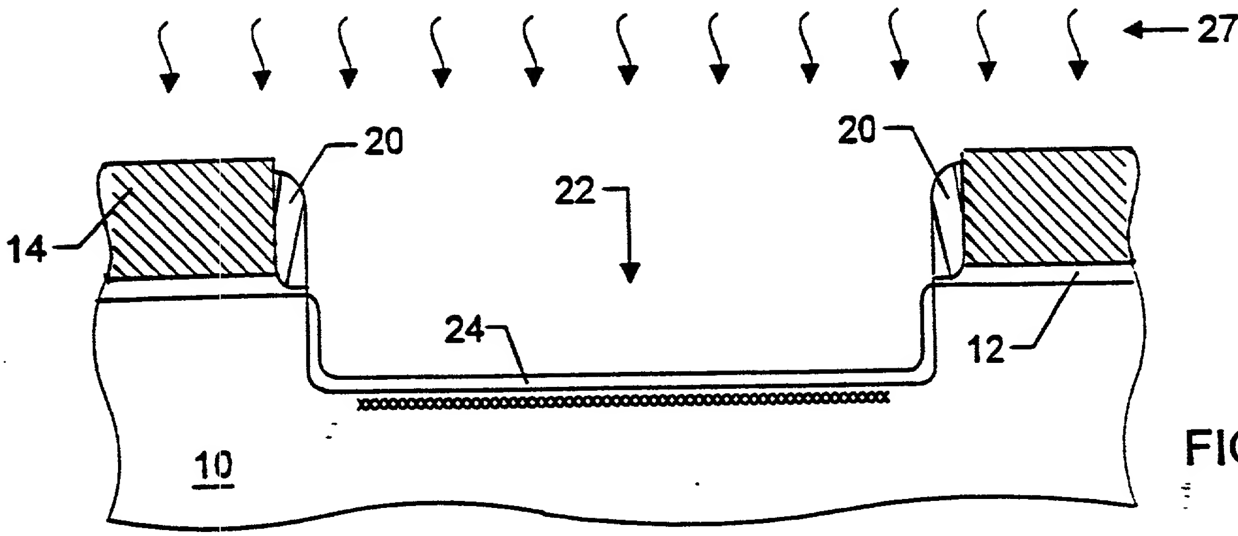

FIG. 8

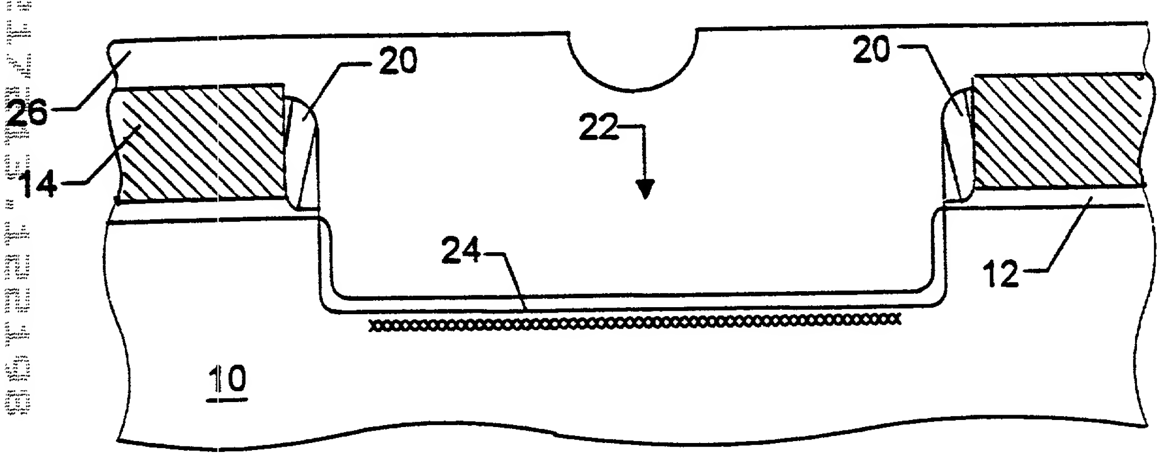

FIG. 9

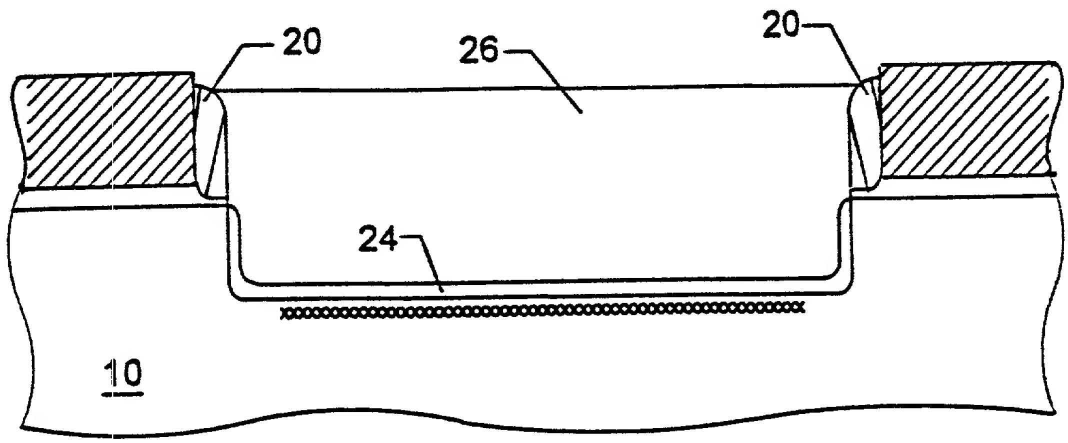

FIG. 10

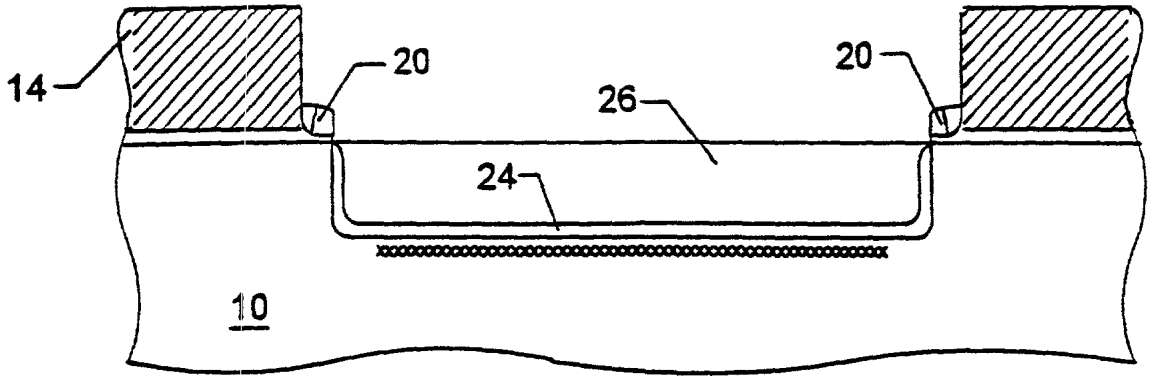

FIG. 11

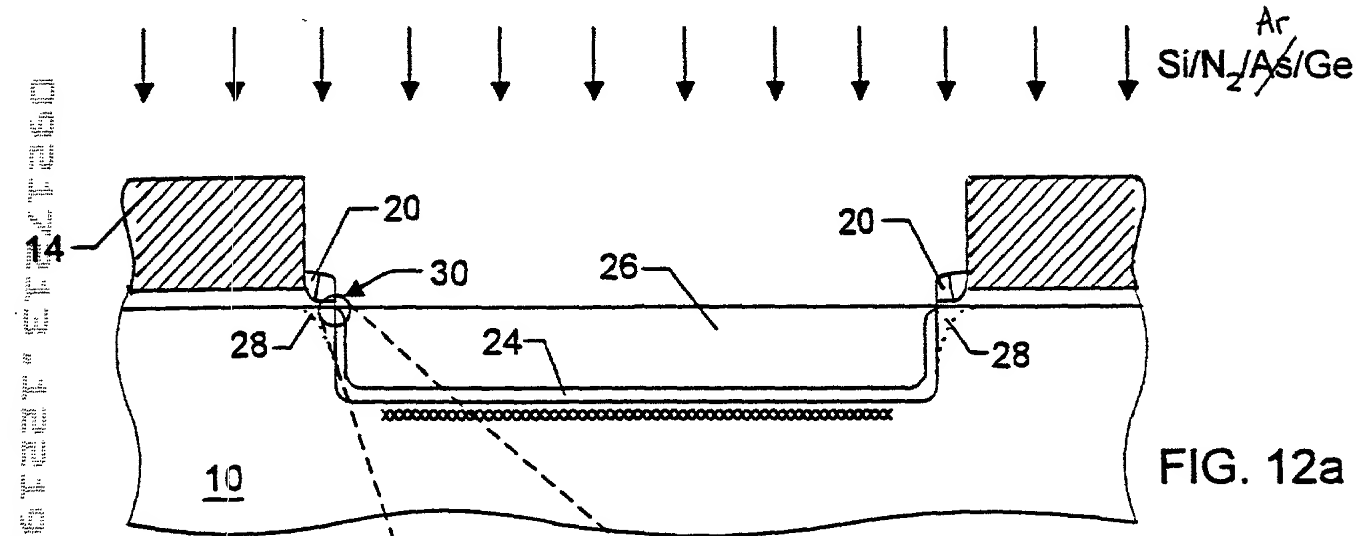

FIG. 12a

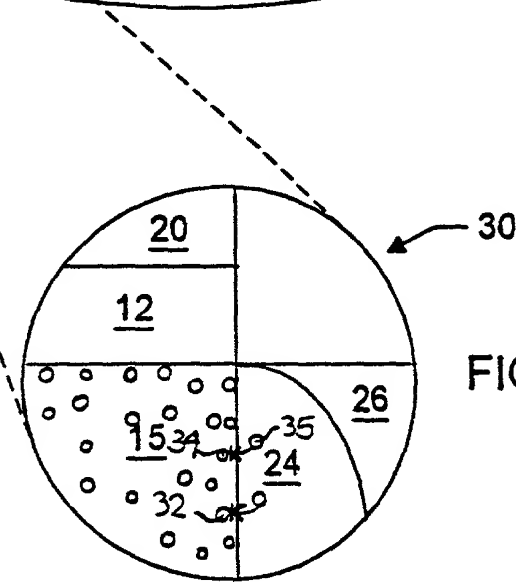

FIG. 12b

Note change to Fig. 12a

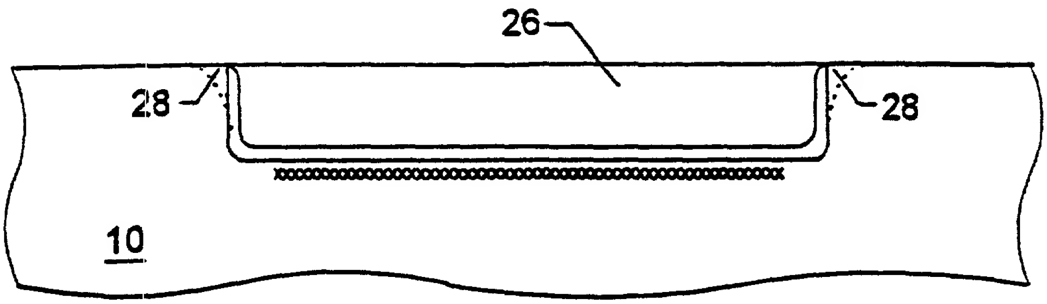

FIG. 13

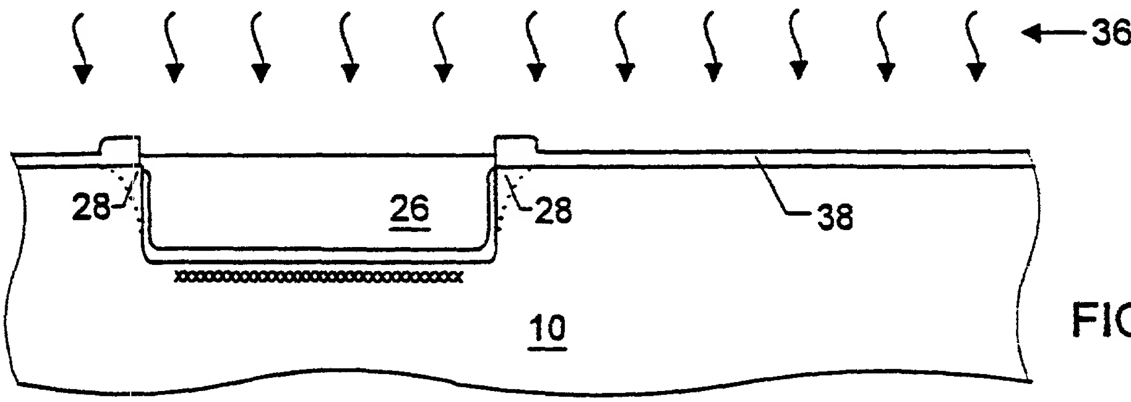

FIG. 14

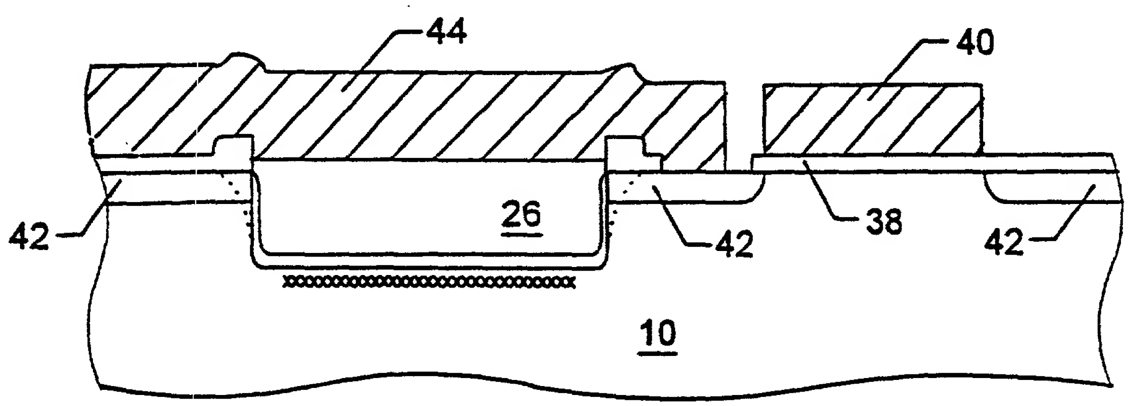

FIG. 15

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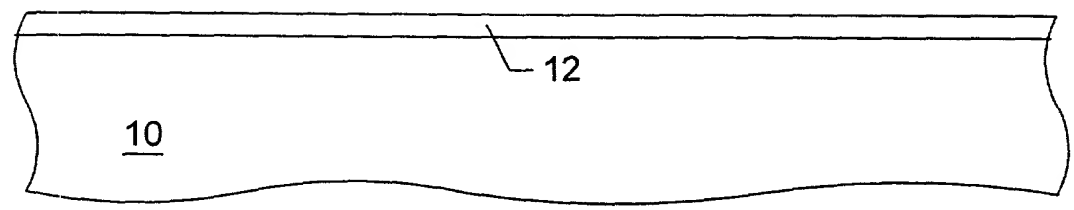
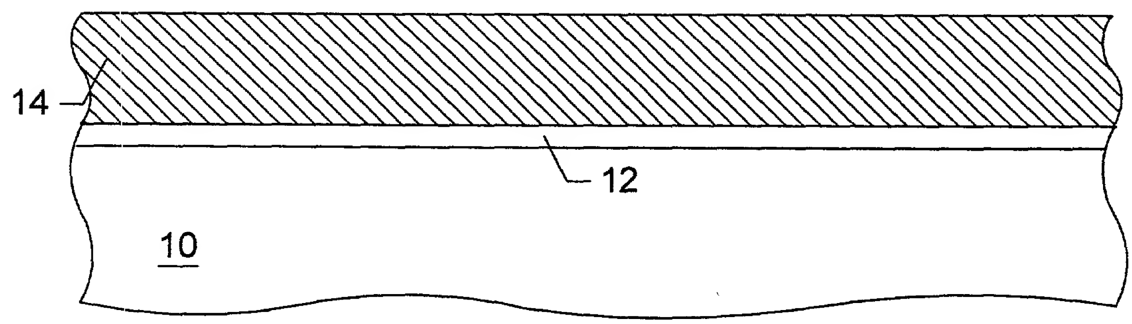


FIG. 1



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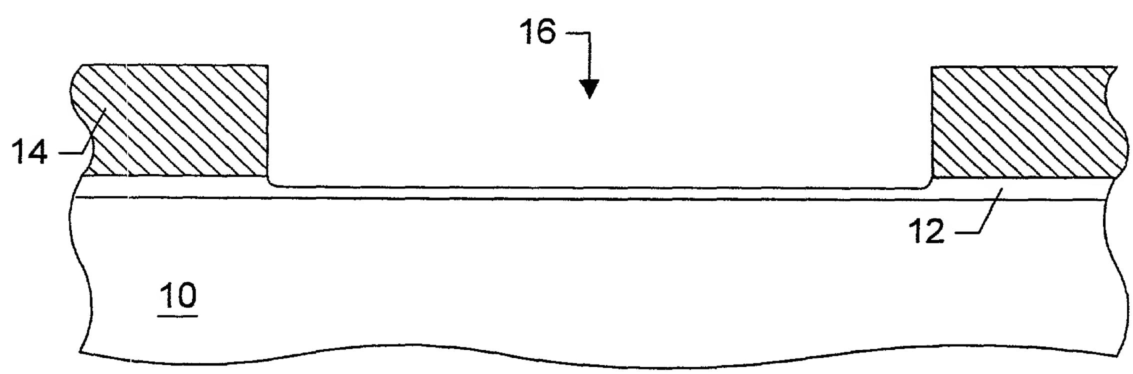

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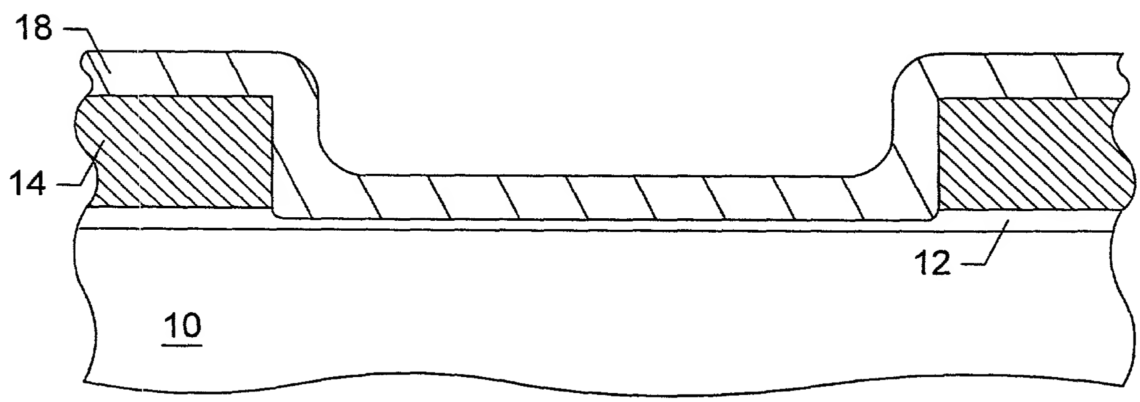

FIG. 4

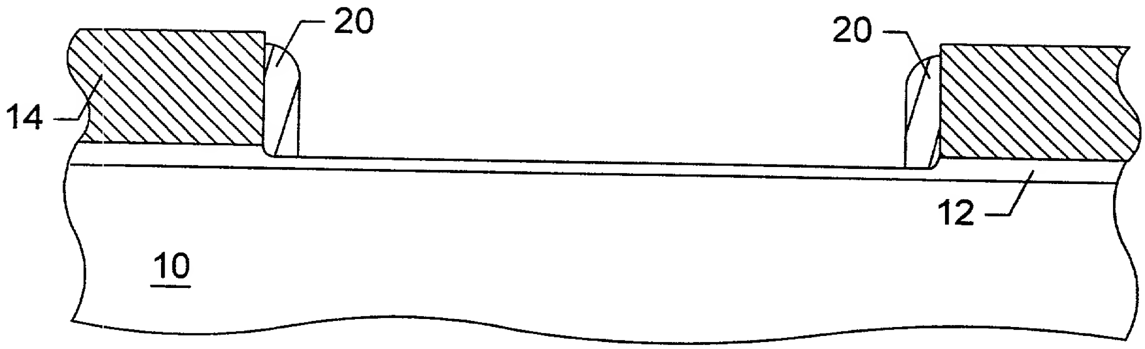

FIG. 5

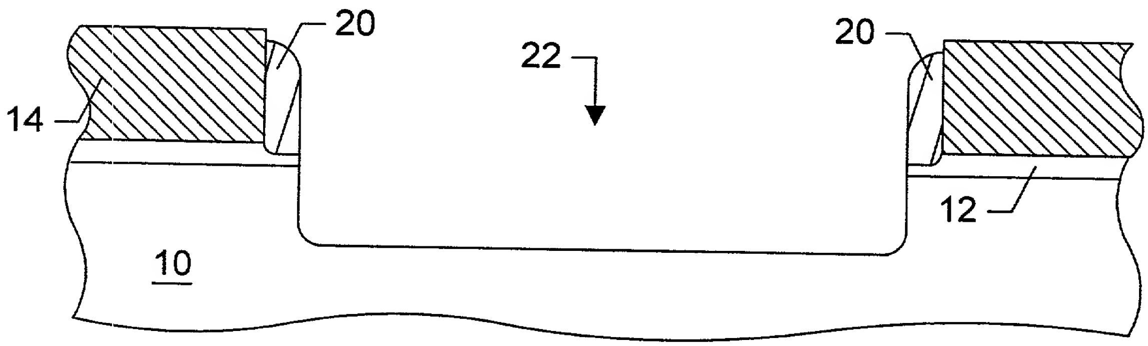

FIG. 6

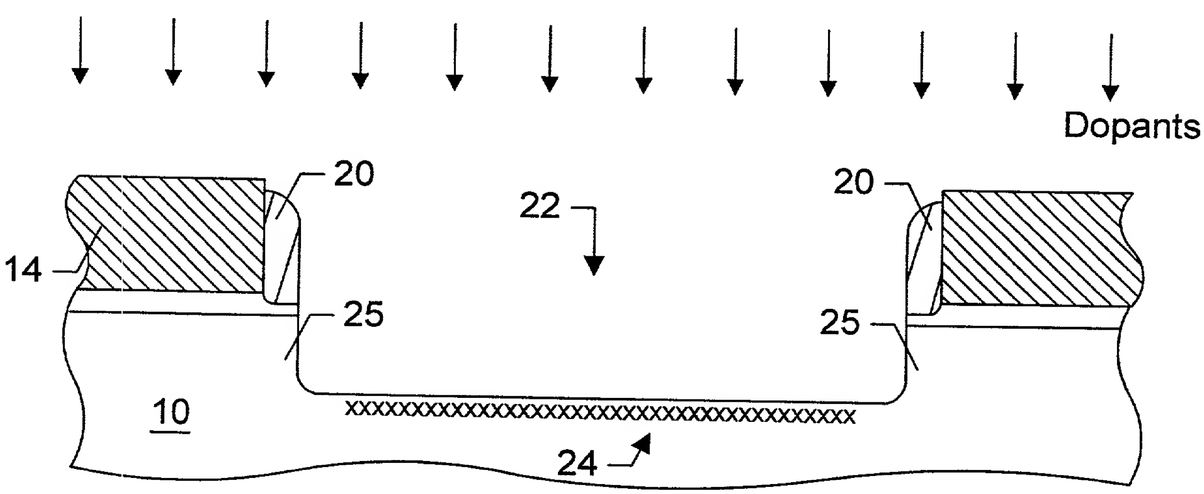

FIG. 7

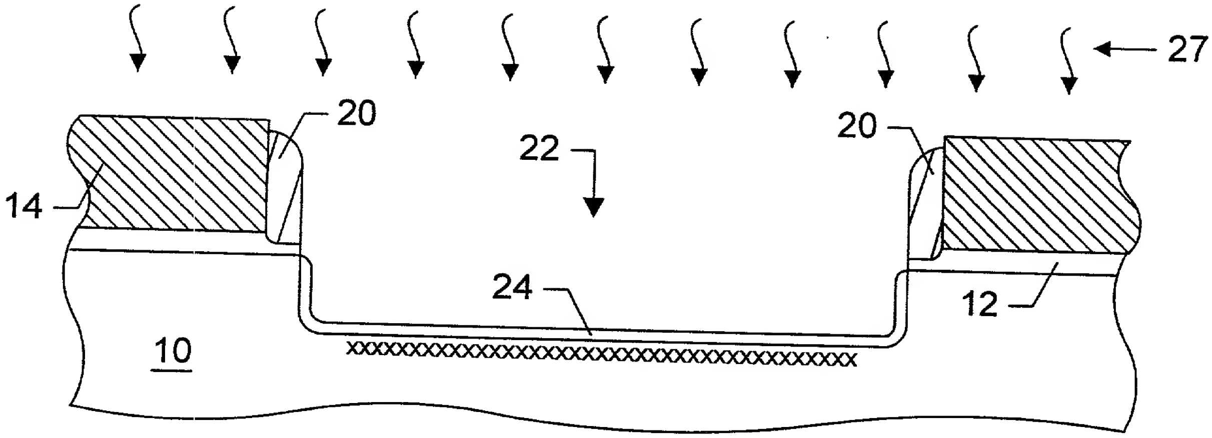

FIG. 8

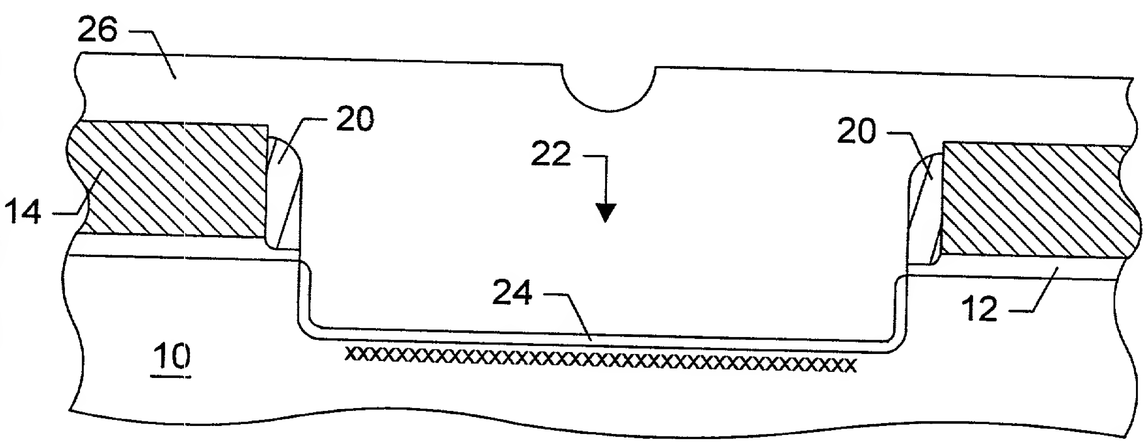

FIG. 9

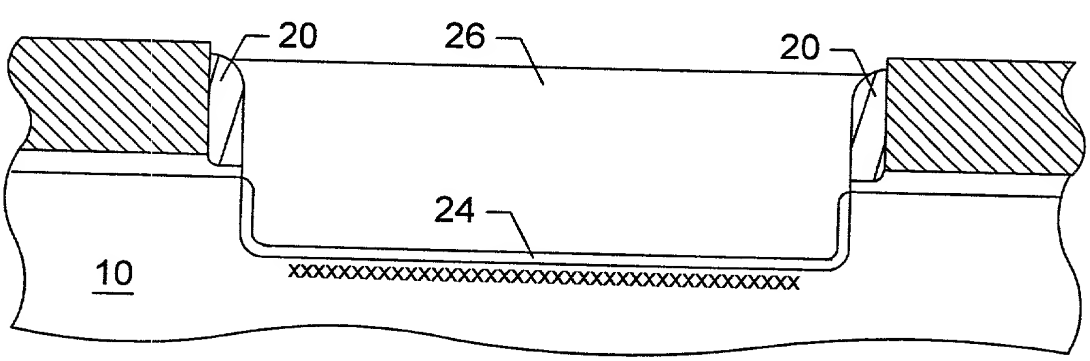

FIG. 10

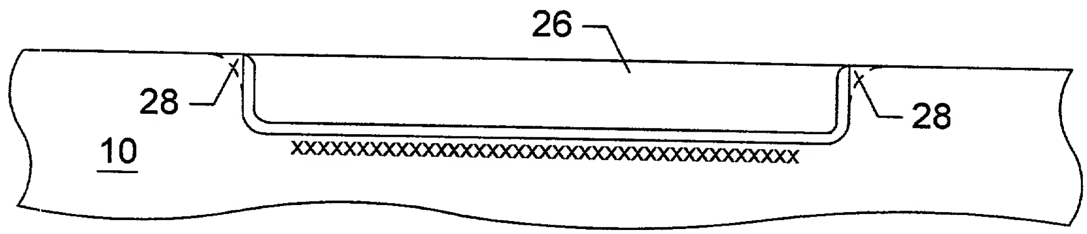

FIG. 13

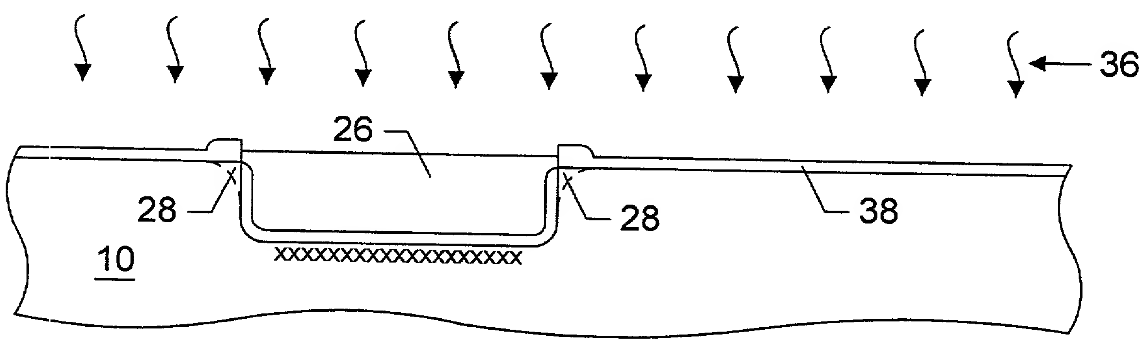

FIG. 14

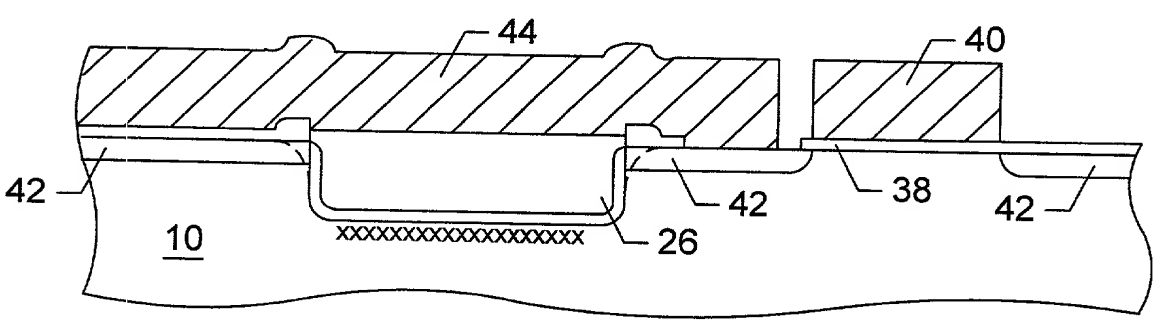

FIG. 15

DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare that:

My residence, post office and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or the below named inventors believe they are the original, first and joint inventors (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled "Semiconductor Fabrication Employing Implantation Of Excess Atoms At The Edges Of A Trench Isolation Structure", the specification of which:

X is attached hereto.
___ was filed on ____________________ as Application Serial No.________________
and was amended on ____________________. (if applicable)

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose to the Patent and Trademark Office all information known to me to be material to patentability of the subject matter claimed in this application, as "materiality" is defined in Title 37, Code of Federal Regulations§ 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, § 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

PRIOR FOREIGN APPLICATION(S)			Priority Claimed
N/A			Yes/No
(Number)	(Country)	(Date Filed)	
N/A			Yes/No
(Number)	(Country)	(Date Filed)	

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose all information known to me to be material to the patentability of the subject matter claimed in this application, as "materiality" is defined in Title 37, Code of Federal Regulations, § 1.56, which become available between the filing date of the prior application and the national or PCT international filing date of this application:

N/A		
(Application Serial No.)	(Filing Date)	(Status)
(Application Serial No.)	(Filing Date)	(Status)

The Assignee hereby revokes any previous Powers of Attorney and appoints Mikio Ishimaru, Reg. No. 27,449; Gerald M. Fisher, Reg. No. 24,599, Vicenzo D. Pitruzzella, Reg. No. 28,656; Richard J. Roddy, Reg. No. 27,688; William D. Zahrt II, Reg. No. 26,070; Charles E. Quarton, Reg. No. 24,825; Louise K. Miller, Reg. No. 36,609; Paul S. Drake, Reg. No. 33,491 and Louis A. Riley, Reg. No. 39,817; each said attorneys being employed by Advanced Micro Devices, Inc.; and Kevin L. Daffer, Reg. No. 34,146, B. Noël Kivlin, Reg. No. 33,929, Jeff C. Hood, Reg. No. 35,198, Eric B. Meyertons, Reg. No. 34,876, Eric A. Stephenson, Reg. No. 38,321; Joseph P. Lally, Reg. No. 38,947; and David A. Rose, Reg. No. 26,223, each said attorneys being members or associates of the firm of Conley, Rose & Tayon, P.C., as attorney or agent for so long as they remain with such company or firm, with full power of substitution and revocation, to prosecute the application, to make alterations and amendments therein, to transact all business in the Patent and Trademark Office in connection therewith, and to receive the Letters Patent.

Please direct all communications as follows:

Kevin L. Daffer
Conley, Rose & Tayon, P.C.
P.O. Box 3267
Houston, Texas 77253-3267
Ph: (512) 476-1400

I hereby declare that all statements made of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Inventor's Full Name: Mark (First) I. (Initial) Gardner (Last)

Inventor's Signature: [signature] Date: 9/2/97

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(Include number,street name, city, state and zip code)

Inventor's Full Name: H. (First) Jim (Initial) Fulford (Last)

Inventor's Signature: [signature] Date: 9/2/97

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Inventor's Full Name: Derick J. Wristers
(First) (Initial) (Last)

Inventor's Signature: ______________ Date: 9/12/97

City and State (or Foreign Country) of Residence: Austin, Texas Citizenship: U.S.A.

Post Office and Residence Address: 1904 Terisu Cove, Austin, Texas 78728
(Include number, street name, city, state and zip code)